CIS*2030: Structure and Application of Microcomputers Computer Science, Fall 2018

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General Description

This course is intended to provide an introduction to the topic of Computer Architecture. Computer

architecture refers to those attributes of a system that are visible to a programmer, or put another

way, those attributes that have a direct impact on the logical execution of a program. As a result

of this course, students will gain insight into the operation of the major components of a computer

system, assembly-language programming, and computer interfacing. The Motorola 68000 has

been selected as the example architecture to study, due to the simplicity and clarity of its

architecture.

Course Outline

Each bullet corresponds to roughly 1-3 weeks of the semester.

• Binary encoding and data representation: number systems, binary arithmetic, complement

arithmetic, ranges, arithmetic overflow, and other code systems

• Basic hardware components, overall architecture and data flow of a typical computer,

Instruction-Set Architecture for M68000

• An assembler language view of the M68000

• Hardware support for high-level language (C) concepts: data structures, loops, conditional

statements, hardware stack, functions, parameter passing, return values, stack frames,

local variables, recursion and re-entrant code.

• Hardware support for Operating Systems: privileged states; exception processing

• Interaction among components: device operation, device control, bus signals, input/output

protocols: polling, interrupts, direct-memory access

Memory Hierarchy and Caching (if time permits)

Fixed- and Floating-Point representations (if time permits)

Textbook

- Mackenzie S., (1995). The 68000 Microprocessor, Prentice-Hall (Required)
- 68KMB Lab Exercises (Provided)

Lectures

There are two sections for this course and there will be three lectures per week for each section: MWF, 8:30am to 9:20am ROZH102, and 1:30pm to 2:20pm, ALEX100. Course notes, reading assignments, etc. will be available on course links.

Course Evaluation

Your final grade will be determined as follows:

Weight	Description	Notes	
20%	Homework Assignments (DD/MM/YY)	Due at beginning of class – Late	
		assignments will not be accepted	
	A1- Hand Out: 07/09/18 – Hand In: 17/09/18	for any reason; however, the	
	A2- Hand Out: 21/09/18 – Hand In: 01/10/18	lowest weight assignment will be	
	A3- Hand Out: 05/10/18 – Hand In: 15/10/18	dropped when calculating your	
	A4- Hand Out: 19/10/18 – Hand In: 29/10/18	final grade	
	A5- Hand Out: 02/11/18 – Hand In: 12/11/18		
30%	Weekly Laboratory Assignments (10)	Labs are not optional. All lab	
		exercises must be completed and	
		submitted to pass the course.	
20%	Midterm	Date: October 26, 1:30pm to	
		2:20pm, in class	
30%	Final Exam	Date: December 4, 11:30am to	
		1:30pm, Room: TBA	

Total Grade = 20%(Homework) + 30%(Labs) + 20%(Midterm) + 30%(Exam)

You must achieve a passing grade on the examination portion of the course (i.e., 22.5 out of 45) and a passing grade (i.e., 50%) on a minimum 9 of 10 lab assignments. Failure to satisfy either of the previous cases results in the following calculation for your final grade: Final Grade = MIN (45, Total Grade).

Teaching Assistants

Teaching Assistants allocated to this course: TBA

All requests for re-grades must be made by email to your marker within one week of an assignment/exam being returned.

Advising hours

• TA advising hours: See course website for dates and times.

A Word of Caution

Needless to say, plagiarism in any form must be dealt with severely. Discussion with fellow students about problems is healthy. However, when answering questions do it yourself. Be original. All cases of academic misconduct are handled by the Dean, in conjunction with the Department Chair. Successive infractions of misconduct affirmed by this process could have consequences as serious as expulsion from the University. (It is your responsibility to acquaint yourself with the definitions and ramifications of academic misconduct as described in the university's undergraduate Calendar.) The risks are sufficiently great that they are not worth taking. If you are having trouble, please see the teaching assistant or the instructor for help.

Lab Schedule for Fall 2018

	MON	TUE	WED	THR	FRI
SEPT					7
	10	11	12	13	first class
	17	18	19	20	21
	LAB 1	LAB 1	LAB 1	LAB 1	LAB 1
	24	25	26	27	28
	LAB 2	LAB 2	LAB 2	LAB 2	LAB 2
OCT	01 LAB 3	02 LAB 3	03 LAB 3	04 LAB 3	05 LAB 3
	08	09	10	11	12
	Holiday	Holiday	LAB 4	LAB 4	LAB 4
	15 LAB 4	16 LAB 4	17 LAB 5	18 LAB 5	19 LAB 5
	22	23	24	25	26
	LAB 5	LAB 5	LAB 6	LAB 6	LAB 6
	29	30	31	1	2
	LAB 6	LAB 6	LAB 7	LAB 7	LAB 7
	5 LAB 7	6 LAB 7	7 LAB 8	8 LAB 8	9 LAB 8
NOV	12	13	14	15	16
	LAB 8	LAB 8	LAB 9	LAB 9	LAB 9
	19 LAB 9	20 LAB 9	21 LAB 10	22 LAB 10	23 LAB 10
	26 LAB 10	27 LAB 10			

Lab Section 0102: Thursday, 8:30am – 11:20am, THRN 3401 Lab Section 0103: Friday, 2:30pm - 5:20pm, THRN 3401 Lab Section 0104: Wednesday, 8:30am – 11:20am, THRN 3401 Lab Section 0105: Monday, 8:30am – 11:20am, THRN 3401 Lab Section 0106: Wednesday, 5:30pm – 8:20pm, THRN 3401 Lab Section 0107: Monday, 2:30pm – 5:20pm, THRN 3401

Lab Section 0101: Tuesday, 8:30am – 11:20am, THRN 3401

Lab Section 0107: Monday, 2:30pm – 5:20pm, THRN 3401 Lab Section 0108: Tuesday, 5:30pm – 8:20pm, THRN 3401 Lab Section 0109: Thursday, 5:30pm – 8:20pm, THRN 3401 Lab Section 0110: Thursday, 2:30pm – 5:20pm, THRN 3401

Lab Section 0111: Monday, 5:30pm-8:20pm THRN 3401

Learning Outcomes

Successfully completing the homework and laboratory assignments in this course will contribute to the following learning outcomes:

- 1. Explain the digital representation of numeric and non-numeric data.
- 2. Identify the main abstractions that exist between programs and the actual hardware they run on, explain why these abstractions exits, and describe how they build upon each other.
- 3. Create assembly-language programs to implement some of the main abstractions and evaluate your program through testing and debugging.
- 4. Implement interfaces with external devices using common input-output strategies.
- 5. Describe the memory hierarchy and list trade-offs.