CIS*3120: Digital Systems I

School of Computer Science
Winter, 2018

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General Course Description

The objectives of this course are to develop skills in the design and analysis of digital logic components and circuits, to make students thoroughly familiar with the basics of gate-level circuit design starting from single gates and building up to complex systems, and to provide exposure to circuit design using computer-aided design tools.

Course Content

Each line corresponds to roughly *one week* of the semester.

- Overview of digital logic design
- Logic gates, DeMorgan's Equivalent Forms, positive and negative logic
- Truth tables, SOP and POS expressions, Karnaugh maps, Quine-McCluskey method
- Arithmetic Circuits: adder, subtractor, carry-lookahead adder
- Generalized ALU design, combinational multiplier
- Steering Logic: multiplexers, de-multiplexers, decoders, encoders
- Comparators, parity generation/detection circuits
- Sequential logic: SR, D, latches, SR, D, JK, T, flip flops, registers
- Finite-State Machines; state minimization
- Up/down counters, ring counters
- Sequential multiplier (datapath and controller)
- Random-Access Memory (RAM): SRAM and DRAM
- Programmable Devices: PROMs, PALs, PLAs, and FPGAs

Textbook

Mano. M. and M. Ciletti (Sixth Edition). *Digital Design*, Pearson.

Lectures

There will be *three* lectures per week: MWF (10:30am – 11:20am) in CRSC 117. Due to the nature of the course material, most of the lecture material will be presented on the chalk board. Therefore, please make sure to attend class regularly. No online notes are available.

Homework

Homework problems will be assigned each Monday and will be due the following Monday at the beginning of class. Solutions will be made available the following week. Late assignments will not be accepted. However, your lowest assignment mark will be dropped when computing your final grade.

Labs

Each week you will be designing and simulating various digital circuits using *LogicWorks* – a Windows based software package. There are 11 lab exercises. You are required to complete and receive a mark for each exercise during your scheduled two-hour weekly lab session. You cannot move between lab sections. Therefore, it is strongly recommended that you prepare for the lab exercise before attending the lab.

Course Evaluation

Weight	Description
5%	Weekly Homework Assignments - *weighted equally* - *start January 8*
20%	Weekly Laboratory Exercises - *weighted equally except for the last lab which is 5%* - *see lab schedule for dates*
30%	Test 1 (15%) - February 16 Test 2 (15%) - March 23
45%	Final Exam (2018/04/13): 2:30pm to 4:30pm (Place: TBA)
Total Grade = 5% (Homework) + 20% (Labs) + 15% (Tests) + 45% (Exam)	

Teaching Assistants (TAs)

- Samuel Opawale <sopawale@uoguelph.ca>
- Elliot Cooper <ecoope07@uoguelph.ca>

Both TAs are responsible for marking in the course. All requests for re-grades must be made by email to the GTA who marked your assignment, lab or test within one week of a marked item being returned.

Advising Hours

Open-door policy; otherwise, please email me to request a specific time. Please do not send questions by email.

A Word of Caution

Needless to say, plagiarism in any form must be dealt with severely. Discussion with fellow students about problems is healthy. However, when answering questions do it yourself. Be original. All cases of academic misconduct are handled by the Dean, in conjunction with the Associate Director of the School. Successive infractions of misconduct affirmed by this process could have consequences as serious as expulsion from the University. *(It is your responsibility to acquaint yourself with the definitions and ramifications of academic misconduct as described in the university's undergraduate Calendar.)* The risks are sufficiently great that they are not worth taking. If you are having trouble, please see the teaching assistant or the instructor for help.

Learning Outcomes

Successfully completing the homework and laboratory assignments in this course will contribute to the following learning outcomes:

1. Understand basic combinational and sequential digital logic.
2. Design and analyze basic/advanced digital circuits.
3. Ability to implement combinational and sequential circuits out of standard TTL parts.
4. Implement finite-state machines as digital circuits.
5. Implement a basic data path and control unit.

Lab Schedule for W18

	MON	TUE	WED	THR	FRI
JAN	8	9	10	11	12
	15 **Lab 1**	16	17 **Lab 1**	18	19
	22 **Lab 2**	23	24 **Lab 2**	25	26
	29 **Lab 3**	30	31 **Lab 3**	1	2
FEB	5 **Lab 4**	6	7 **Lab 4**	8	9
	12 **Lab 5**	13	14 **Lab 5**	15	16
Winter Break	19 ☺	20 ☺	21 ☺	22 ☺	23 ☺
	26 **Lab 6**	27	28 **Lab 6**	1	2
MAR	5 **Lab 7**	6	7 **Lab 7**	8	9
	12 **Lab 8**	13	14 **Lab 8**	15	16
	19 **Lab 9**	20	21 **Lab 9**	22	23
	26 **Lab 10**	27	28 **Lab 10**	29	30 ***no class*** ☺
APR	2 **Lab 11**	3	4 **Lab 11**	5	6 ***last class*** ☺

Lab Times:

- Monday, 3:30pm – 5:20pm, THRN 2420
- Wednesday, 8:30am – 10:20am, THRN 2420