CIS*3120: Digital Systems I

School of Computer Science
Winter, 2023

Instructor: G. Grewal
Office: 2208 Reynolds
Phone: x52630
E-mail: ggrewal@uoguelph.ca
CourseLink: https://courselink.uoguelph.ca

General Course Description

The objectives of this course are to develop skills in the design and analysis of digital logic components and circuits, to make students thoroughly familiar with the basics of gate-level circuit design starting from single gates and building up to complex systems, and to provide exposure to circuit design using a schematic entry based computer-aided design tool.

Course Content

Each line corresponds to roughly *one week* of the semester.

- Overview of digital logic design
- Logic gates, DeMorgan's Equivalent Forms, positive and negative logic
- Truth tables, SOP and POS expressions, Karnaugh maps, Quine-McCluskey method
- Arithmetic Circuits: adder, subtractor, carry-lookahead adder
- Generalized ALU design, combinational multiplier
- Steering Logic: multiplexers, de-multiplexers, decoders, encoders
- Comparators, parity generation/detection circuits
- Sequential logic: SR, D, latches, SR, D, JK, T, flip flops, registers
- Finite-State Machines; state minimization
- Up/down counters, ring counters
- Sequential multiplier (datapath and controller)
- Random-Access Memory (RAM): SRAM and DRAM
- Programmable Devices: PROMs, PALs, PLAs, and FPGAs

Textbook

Mano. M. and M. Ciletti (2015-2018). *Digital Design*, Pearson.

Lectures

There will be *three* lectures per week: MWF (9:30am – 10:20am) in CRSC 117. Due to the nature of the course material, most of the lecture material will be presented on the chalk board. Therefore, please make sure to attend class regularly. No online notes are available.

Homework

Homework problems will be assigned each Monday and will be due the following Monday at the *beginning* of class. Solutions will be made available after class. Late assignments will not be accepted. However, your lowest assignment mark will be dropped when computing your final grade.

Laboratory Exercises

Each week you will be designing and simulating various digital circuits using *LogicWorks* – a Windows based software package. You are required to complete and receive a mark for each exercise *during* your scheduled two-hour weekly lab session. Late lab assignments will not be accepted. Also, you cannot move between lab sections. Therefore, it is strongly recommended that you prepare for each lab exercise before attending the lab.

Course Evaluation

Weight	Description
11%	Weekly Homework Assignments - *weighted equally* - *start January 9*
29%	Weekly Laboratory Exercises - *1-10 (2%), 11 (9%)* - *see lab schedule for dates*
30%	Test 1 (15%) - February 17 (in class) Test 2 (15%) - March 24 (in class)
30%	Final Exam - April 20, 7-9pm (location TBD)

Graduate Teaching Assistants

Abbas Yazinejad is responsible for the marking the lab portion of the course, while Mahmoud Hazari is responsible for marking the homework portion of the course. Contact information for both these individuals can be found on CourseLink. All requests for re-grades must be made by email to the appropriate teaching assistant within 5 working days from the online posting of assignment grades. Generally, work commitments will not constitute grounds for academic consideration; this includes heavy workloads or assignments and tests in other courses.

Advising Hours

Open-door policy; otherwise, please email me to request a specific time. Please do not send questions by email. If you wish to meet with one of the teaching assistants, please contact them via email to arrange a meeting date and time.

A Word of Caution

Needless to say, plagiarism in any form must be dealt with severely. Discussion with fellow students about problems is healthy. However, when answering questions do it yourself. Be original. All cases of academic misconduct are handled by the Dean, in conjunction with the

Associate Director of the School. Successive infractions of misconduct affirmed by this process could have consequences as serious as expulsion from the University. *(It is your responsibility to acquaint yourself with the definitions and ramifications of academic misconduct as described in the university's undergraduate Calendar.)* The risks are sufficiently great that they are not worth taking. If you are having trouble, please see the teaching assistant or the instructor for help.

Lab Schedule for W23

	MON	TUE	WED	THR	FRI
JANUARY	9	10	11	12	13
	16 **Lab 1**	17	18	19 **Lab 1**	20
	23 **Lab 2**	24	25	26 **Lab 2**	27
FEBUARY	30 **Lab 3**	31	1	2 **Lab 3**	3
	6 **Lab 4**	7	8	9 **Lab 4**	10
	13 **Lab 5**	14	15	16 **Lab 5**	17 **TEST 1**
Winter Holiday	20 ☺	21 ☺	22 ☺	23 ☺	24 ☺
	27 **Lab 6**	28	1	2 **Lab 6**	3
MARCH	6 **Lab 7**	7	8	9 **Lab 7**	**10**
	13 **Lab 8**	14	15	16 **Lab 8**	17
	20 **Lab 9**	21	22	23 **Lab 9**	24 **TEST 2**
	27 **Lab 10**	28	29	30 **Lab 10**	31
APRIL	3 **Lab 11**	4	5	6 **Lab 11**	7 **Holiday**
	10 ☺ **Last Class**				

Lab Times:

- Monday 2:30pm – 4:20pm (Section 0101)
- Thursday 2:30pm – 4:20pm (Section 0102)

Place: THRN 2418